# IntelliHome: An FPGA-Based Implementation of an EEG-Controlled Smart Home

## TEAM #CE05 CONTRIBUTORS



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## SPONSORS


1. National Science Foundation


## REQUIREMENTS

1. Detects electrical activity from the user's brain
2. Processes and classifies electrical activity
3. Headset is locally portable, able to be moved throughout a home
4. Controls user's radio with relaxed and focused brain states
5. Signals are processed in less than 1 ms

## HARDWARE & BUDGET

| Component | Price |
|---|---|
| KC705 Development Board | $1,695.00 |
| PmodUSBUART Bridge | $ 16.03 |
| USB to Micro USB Adapter | $ 5.34 |
| XM105 FMC Card | $ 185.13 |
| EEG Headset | - |
| OpenBCI Cyton Board | $ 499.99 |
| Controllable Outlet Power Relay (x2) | $ 49.90 |
| Lamp | $ 15.99 |
| Radio | $ 14.99 |
| Total | $2,482.37 |
| Total Responsible | $ 271.39 |

## STANDARDS

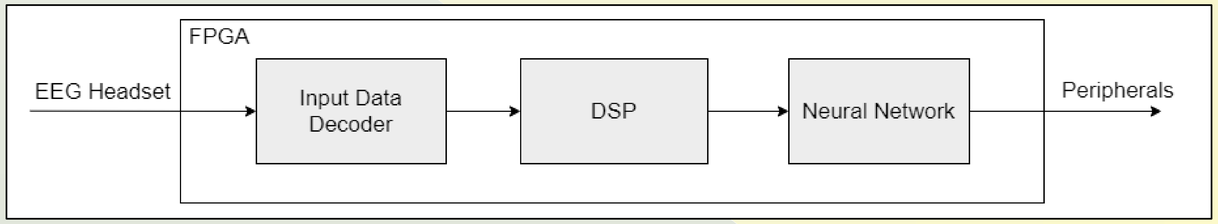
1. Intel Avalon Interface Specifications
2. Universal Asynchronous Receiver-Transmitter (UART)
3. Sitronix-ST7066U (LCD Spec)

## PROBLEM STATEMENT

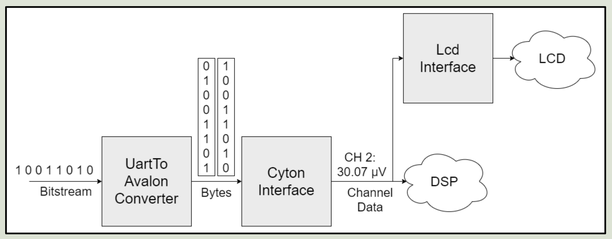
Every year, new technology arises to make people's lives easier and simpler. It is becoming increasingly common for people to utilize voice activated devices to control features in their home. However, these devices require active command by a human to use. If a device existed that could know when a specific feature was needed without receiving a conscious command, a person's environment could be tailored entirely to their needs, increasing quality of life.

## SOLUTION

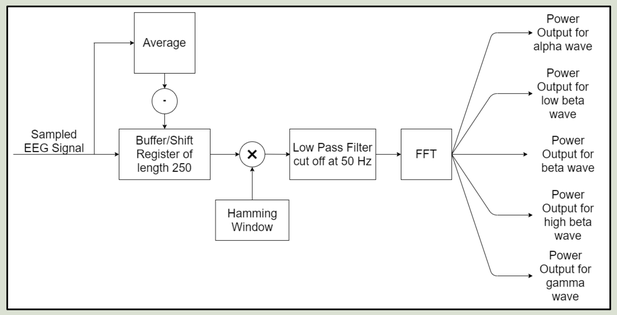
The solution is to use an electroencephalogram (EEG) to collect electrical brain data and analyze them on an FPGA. The below diagram is a basic overview of the project architecture. Raw EEG data will be passed to the FPGA. The data is received in the form of serial bits and needs to first be decoded into usable data. Digital Signal Processing (DSP) techniques are then needed to extract features. Once the data has been processed, it will be passed into a neural network for classification allowing control of peripherals.



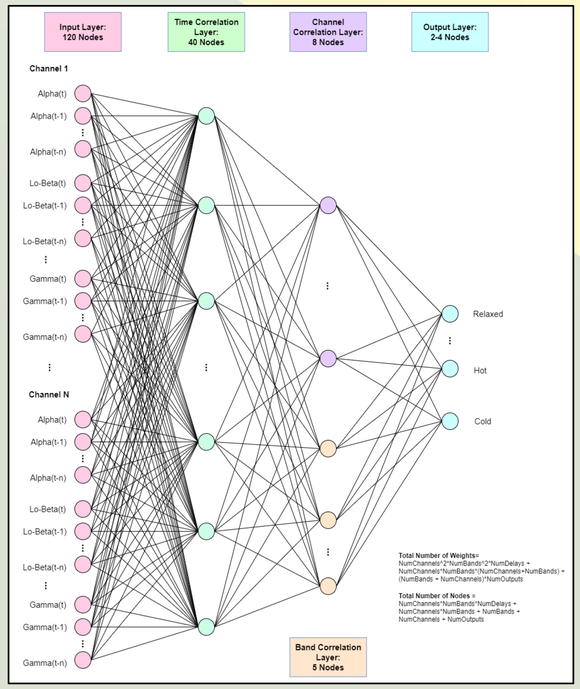

## INPUT DATA DECODER




## DIGITAL SIGNAL PROCESSING




## NEURAL NETWORK




## DEVELOPMENT AND TESTING PROCESS:

1. MATLAB design & testing
2. VHDL component implementation
3. VHDL verification via simulation
4. FPGA component build (if applicable)
5. Test on hardware (if applicable)
6. Next component, back to step 1
7. Link components in top level wrapper
8. VHDL verification via simulation
9. Test on hardware with real-time data

## CHALLENGES

1. No experience with Real-Time DSP.
   **Solution**: Downloaded textbook and worked through content.
2. Communication between FPGA and EEG was not straight-forward or well documented.
   **Solution**: Interpreted Python libraries for Cyton board to determine design
1. No experience with Neural Networks.
   **Solution**: Followed YouTube tutorials and made practice neural networks.

## CONCLUSIONS

1. A proof of concept for the components of an EEG controlled smart home on an FPGA has been completed
2. A neural network that is small enough to fit on many FPGAs was effectively designed to categorize EEG signals. Size: 88,304 Flip Flops
3. Necessary DSP and data decoder was designed

## FUTURE WORK

A proof of concept for the components was completed. Next steps include implementing the DSP and Neural Network design in VHDL and testing on the FPGA.

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